WHAT IS CLAIMED IS:

1. A method of driving a phase detector circuit, the phase detector circuit used to determine a phase difference between a recovered clock and a bitstream, the method comprising:

receiving a first clock phase signal derived from the recovered clock;

receiving a second clock phase signal derived from the recovered clock;

providing access to a constant current circuit in response to a logical combination of the first clock phase signal and the second clock phase signal; and

conducting current between the constant current circuit and the first phase detector circuit.

2. The method as defined in Claim 1, further comprising deactivating access to the constant current circuit in response to the first clock phase signal and the second clock phase signal being at second corresponding states.

3. The method as defined in Claim 1, further comprising AC coupling the constant current circuit to the first clock signal.

4. The method as defined in Claim 1, further comprising sinking current from the first phase detector circuit to allow the phase detector circuit to sink current from the first capacitor.

5. The method as defined in Claim 1, further comprising enabling the constant current circuit in response to the first clock phase signal and the second clock phase signal being at the same state.

6. A phase detector driver circuit configured to drive a phase detector circuit, the phase detector circuit used to determine a phase difference between a recovered clock and a bitstream, the phase detector driver circuit comprising:

a first clock phase signal derived from the recovered clock;

a second clock phase signal derived from the recovered clock;

a constant current circuit coupled to the first clock phase signal and the second clock phase signal, wherein the constant current circuit is enabled and disabled at least partly in response to at least one of the first clock signal and the second clock signal; and

a current steering circuit having a first terminal coupled to the constant current circuit, a second terminal coupled to a first phase detector capacitor, a third terminal coupled to a second phase detector capacitor, and at least a fourth terminal coupled to the bitstream, wherein the steering circuit steers current between the constant current circuit and the first phase detector capacitor in response to a bitstream bit being at a first logic level, and wherein the steering circuit steers current between the constant current circuit and the second phase detector capacitor in response to a bitstream bit being at a second logic level different than the first logic level.

7. The phase detector driver circuit as defined in Claim 6, wherein the constant current circuit is AC coupled to the first clock signal and the second clock signal.

8. The phase detector driver circuit as defined in Claim 6, wherein the constant current circuit includes a constant current sink circuit that sinks current to thereby selectively discharge the first and the second phase detector capacitors.

9. The phase detector driver circuit as defined in Claim 6, wherein the constant current circuit further comprises an enable circuit that provides access to a constant current sink circuit in response to both the first clock signal and the second clock signal being at the same state.

10. The phase detector driver circuit as defined in Claim 6, wherein the constant current circuit further comprises an enable circuit that disables access to a constant current sink circuit in response to the first clock signal and the second clock signal being at different logic states.

11. The phase detector driver circuit as defined in Claim 6, wherein the phase detector driver circuit is fabricated from silicon-germanium.

12. A network interface circuit, comprising:

a first network interface port configured to receive a bitstream from a network; and

a phase detector driver configured to drive a phase detector circuit, the phase detector circuit used to determine a phase difference between a clock and the bitstream, the phase detector driver circuit comprising:

a first clock phase signal based on the clock;

a second clock phase signal based on the clock;

a constant current circuit coupled to the first clock phase signal and the second clock phase signal, wherein the constant current circuit is enabled and is disabled at least partly in response to at least one of the first clock signal and the second clock signal; and

a current steering circuit having a first terminal coupled to the constant current circuit, a second terminal coupled to a first phase detector capacitor, a third terminal coupled to a second phase detector capacitor, and at least a fourth terminal coupled to the bitstream, wherein the steering circuit steers current between the constant current circuit and the first phase detector capacitor in response to a first bitstream bit being at a first logic level, and wherein the steering circuit steers current between the constant current circuit and the second phase detector capacitor in response to a second bitstream bit being at a second logic level different than the first logic level.

13. The network interface circuit as defined in Claim 12, wherein the constant current circuit includes a first transistor AC coupled to the first clock phase signal and a second transistor AC coupled to the second clock phase signal, wherein the first transistor and the second transistor disable a current from flowing from the first phase detector capacitor and the second phase detector capacitor when the first clock phase signal and the second clock phase signal are at the same state.

14. The network interface circuit as defined in Claim 12, wherein the current steering circuit further comprises a bipolar junction transistor coupled to the first, second and fourth terminals, wherein the bipolar junction transistor is used to provide a current path between the first phase detector capacitor and the constant current circuit.

15. The network interface circuit as defined in Claim 12, wherein the network interface circuit is fabricated from silicon-germanium.

16. A method of networking systems using a bitstream, comprising:

receiving serial data from a network at a first network port;

generating a first clock having at least a first phase and a second phase;

causing a constant current to flow in a first path at least in response to at least one state of the first phase and the second phase;

steering current through the first path from a first phase detector storage device in response to a first serial data bit; and

steering current through the first path from a second phase detector storage device in response to a second serial data bit.

17. The method as defined in Claim 16, wherein the network is a SONET network.

18. The method as defined in Claim 16, wherein the first clock is a recovered clock whose frequency is at least in part varied in response to a bit rate of the serial data.

19. The method as defined in Claim 16, wherein the first serial bit has a different logic level than the second serial bit.

20. The method as defined in Claim 16, wherein the first and second phase detector storage devices are capacitors.

21. The method as defined in Claim 16, further comprising AC coupling a signal line carrying the first phase to a constant current sink circuit used to cause constant current to flow in the first path.